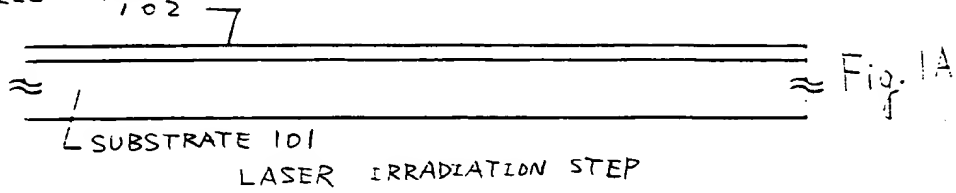
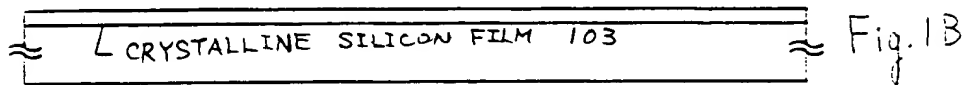


CRYSTALLIZATION STEP

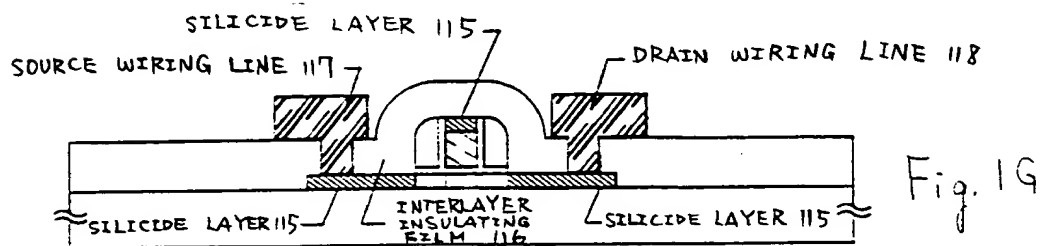
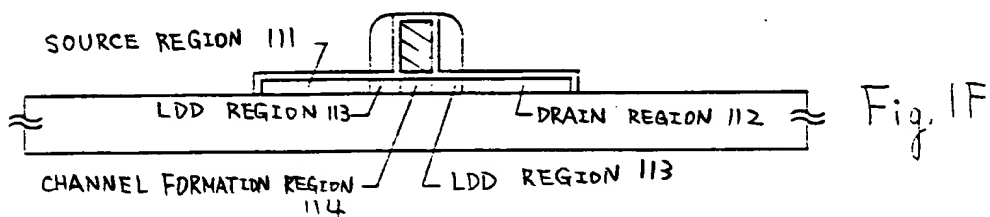
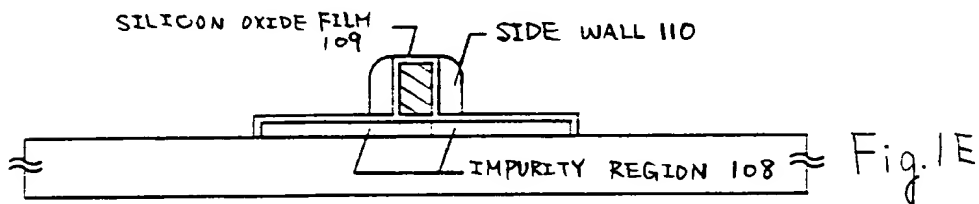
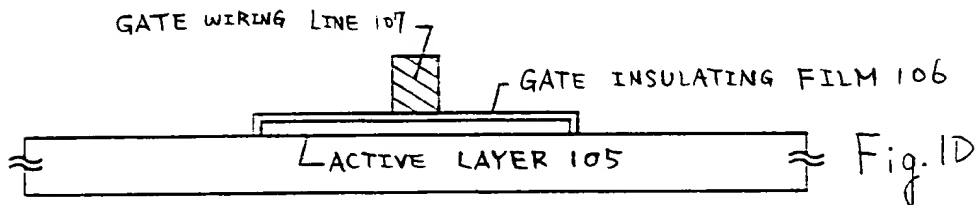
CRYSTALLINE
SILICON FILM
102

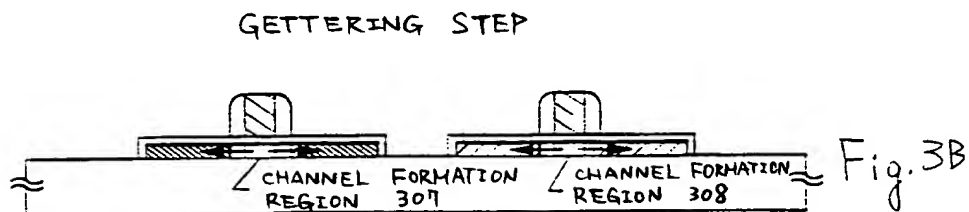
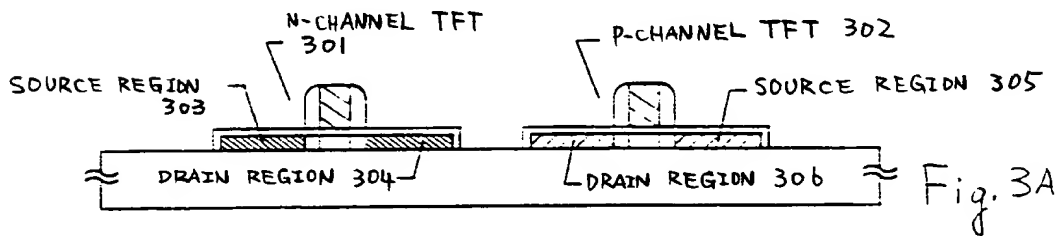
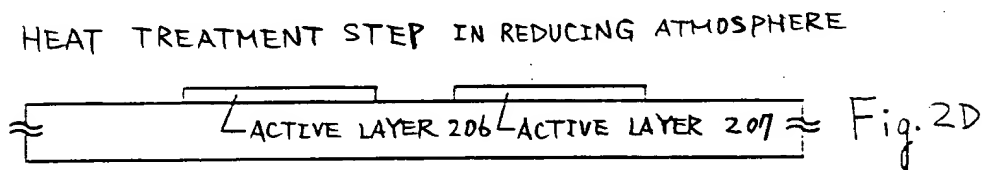
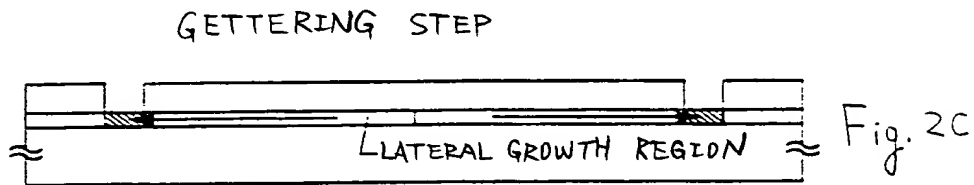
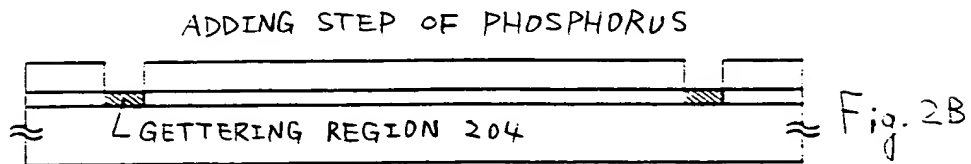
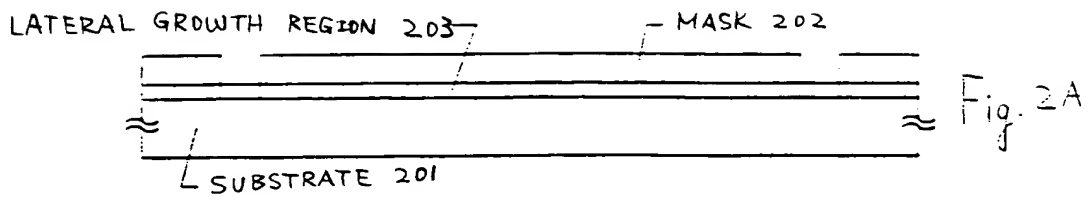


LASER IRRADIATION STEP



HEAT TREATMENT STEP IN REDUCING ATMOSPHERE





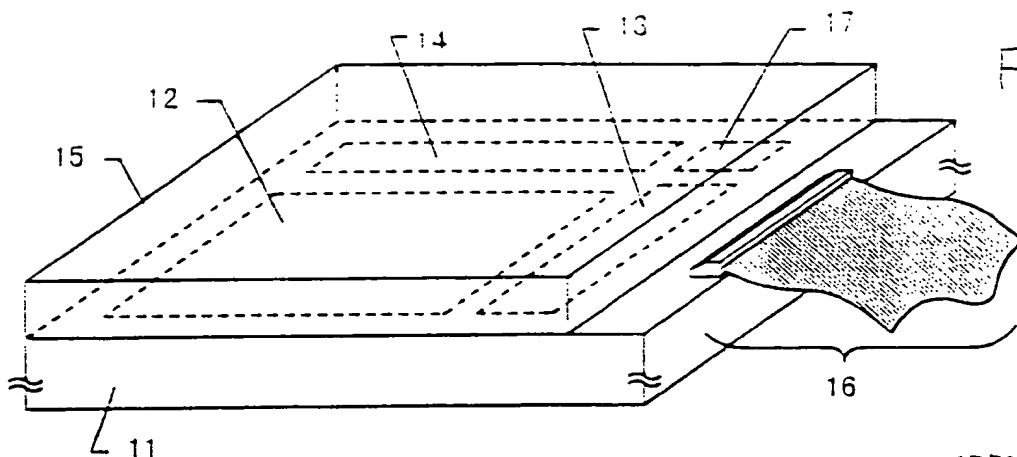


Fig. 4A

- 11: SUBSTRATE HAVING INSULATING SURFACE 12: PIXEL MATRIX CIRCUIT
 13: SOURCE DRIVER CIRCUIT 14: GATE DRIVER CIRCUIT
 15: OPPOSITE SUBSTRATE 16: FPC 17: SIGNAL PROCESSING CIRCUIT

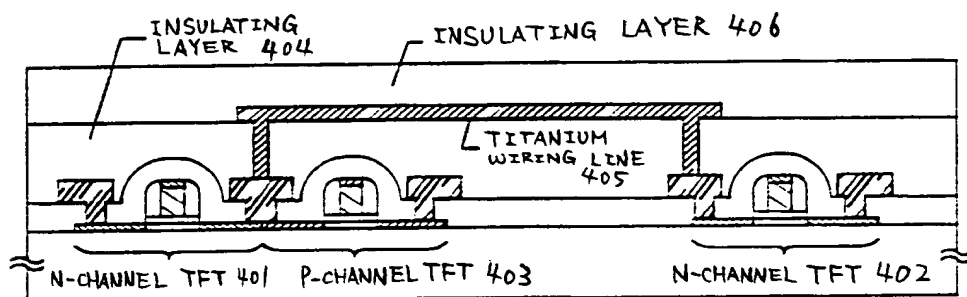


Fig. 4B

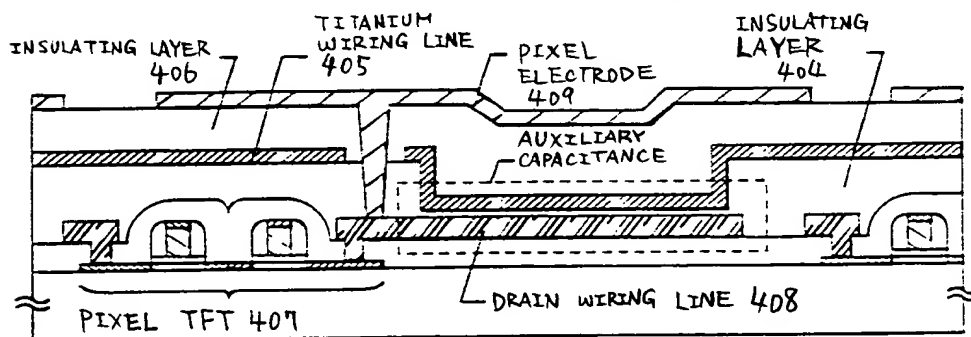


Fig. 4C

662023660

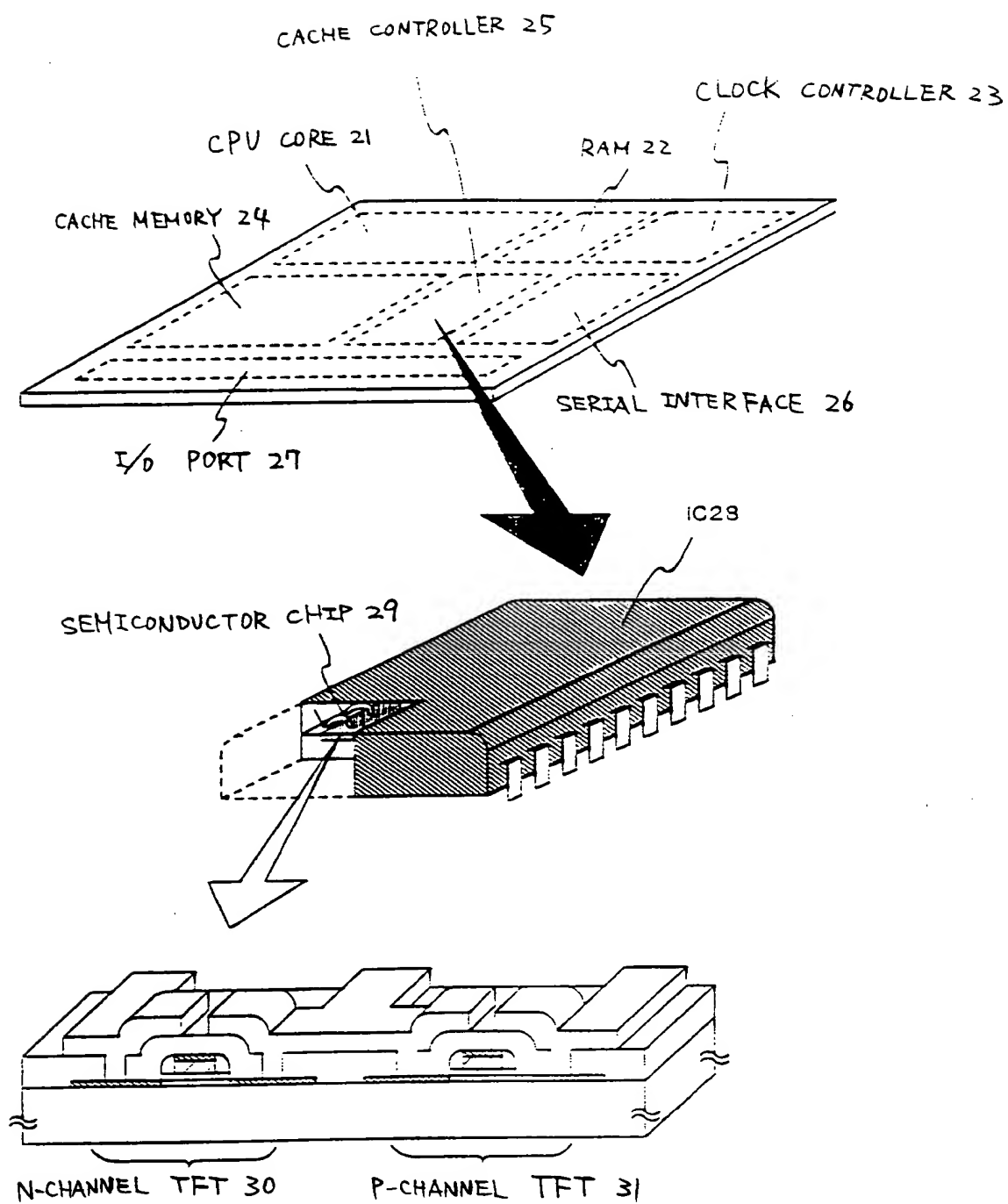
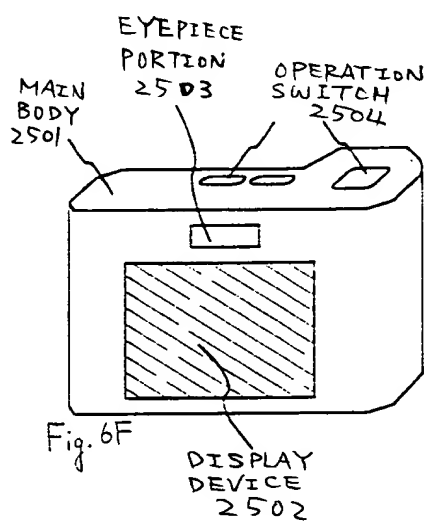
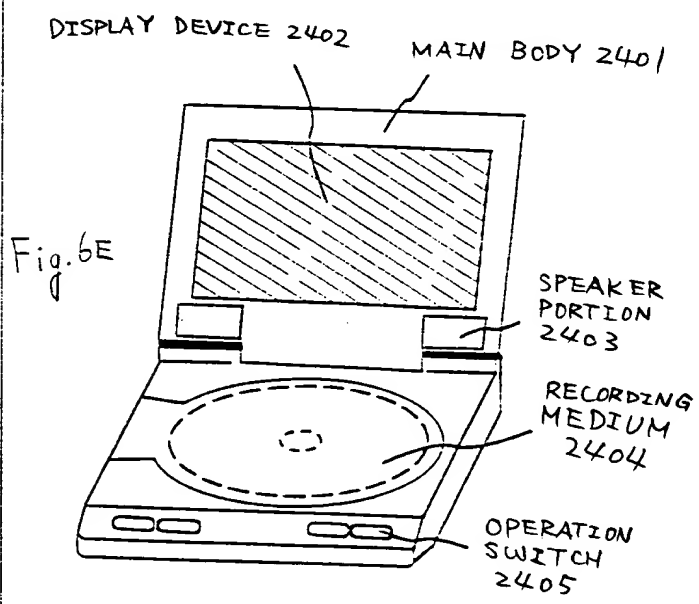
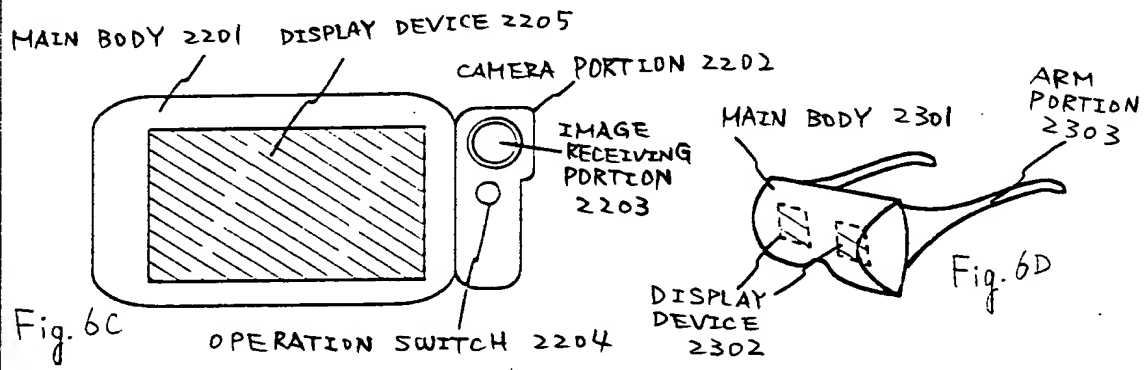
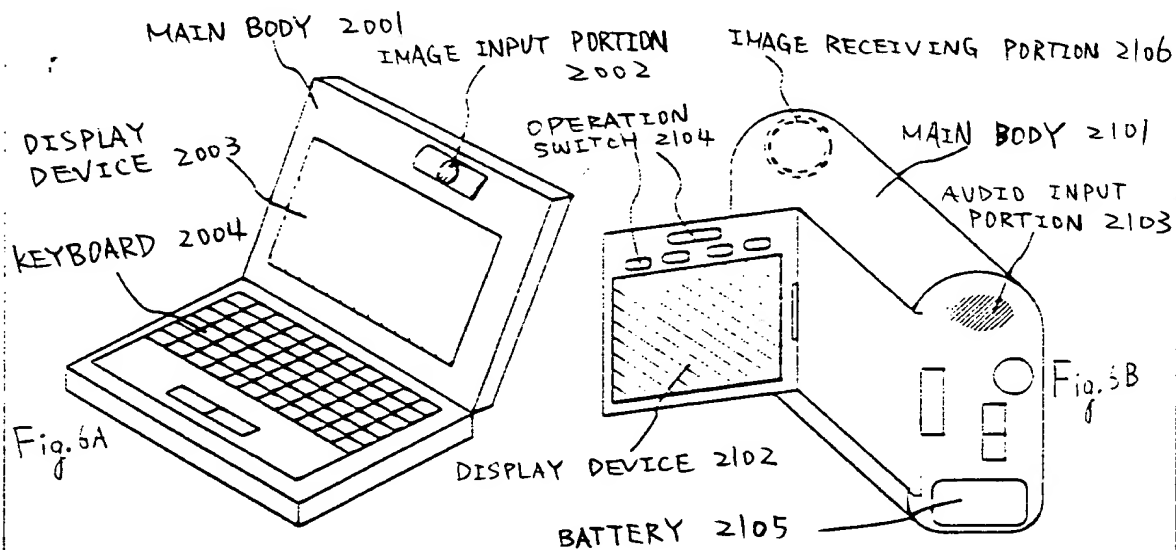


Fig. 5



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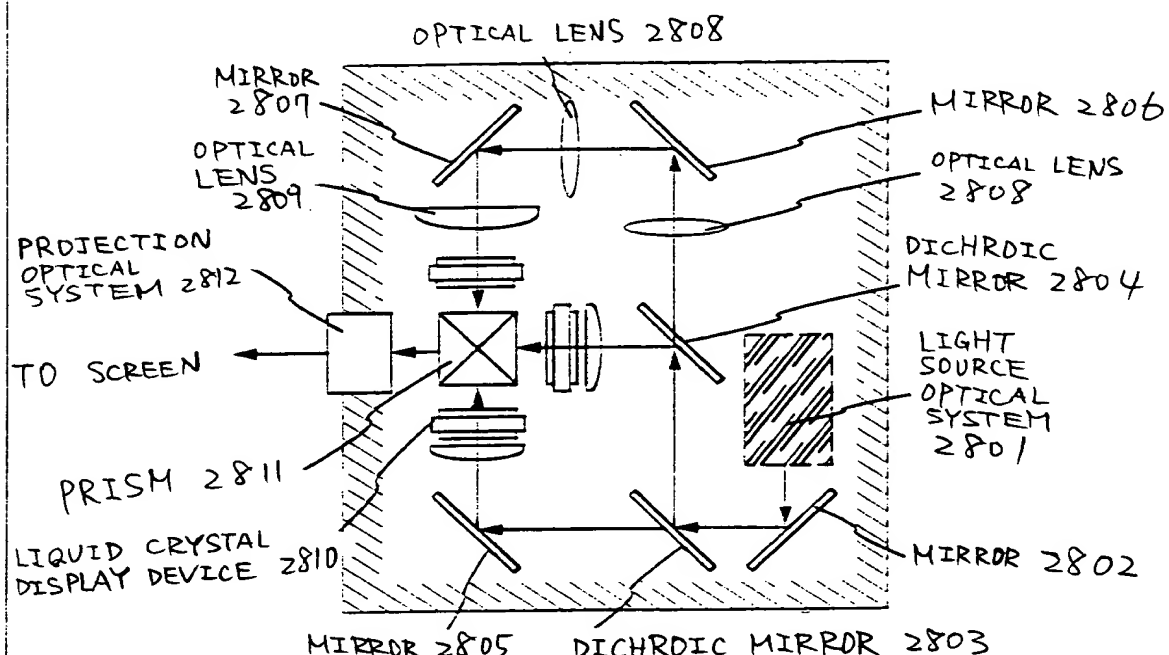
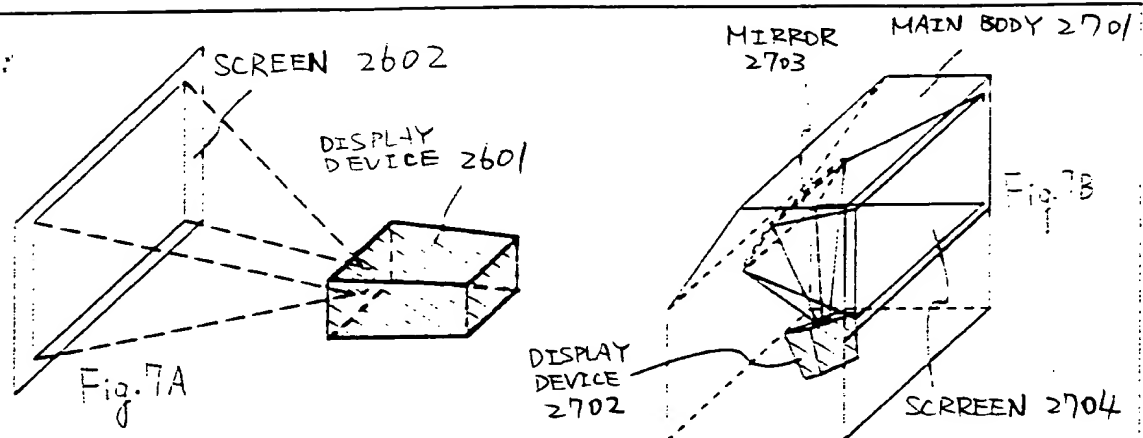


Fig. 7C DISPLAY DEVICE (THREE-PLATE TYPE)

SYNTHESIS PRISM 2815

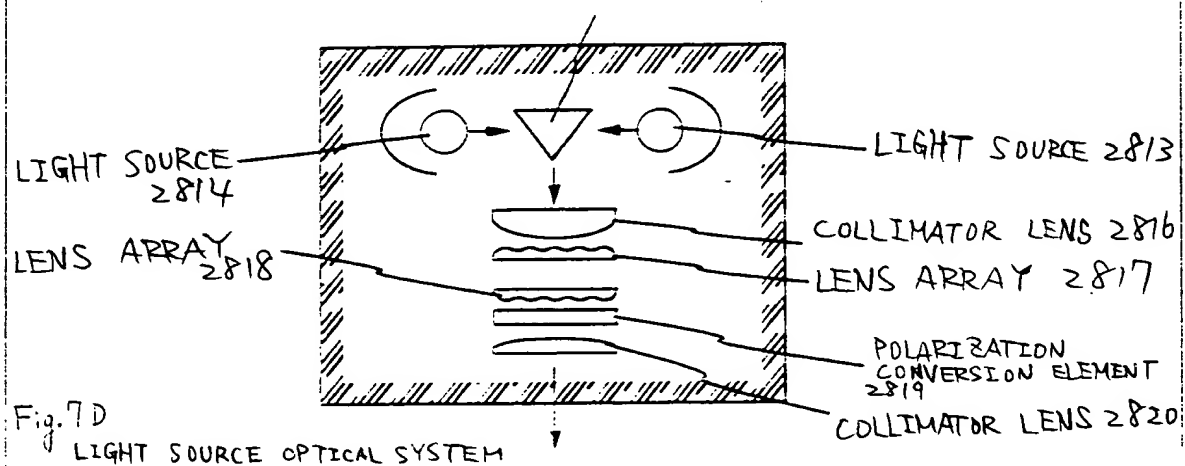


Fig. 7D LIGHT SOURCE OPTICAL SYSTEM

6622923600

DIFFRACTION
SPOT 1201

1203

Fig. 3A

CENTER POINT OF BEAM IRRADIATION AREA 1202

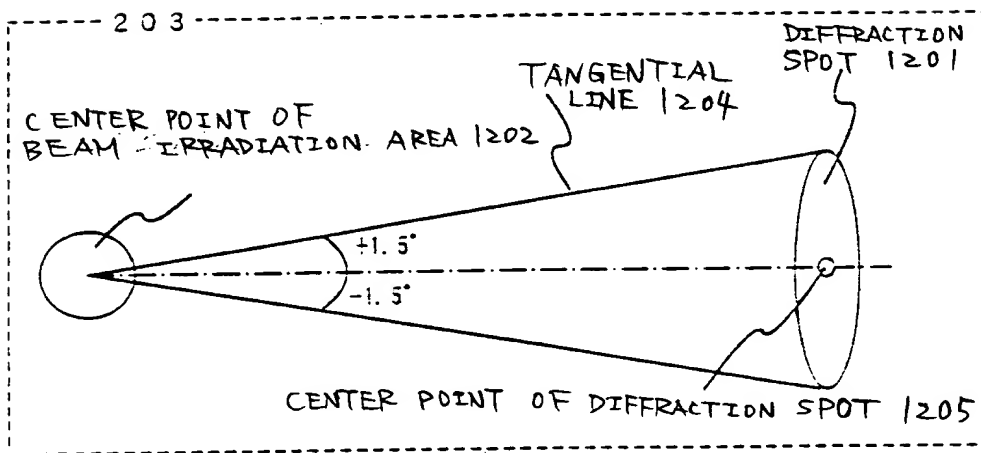
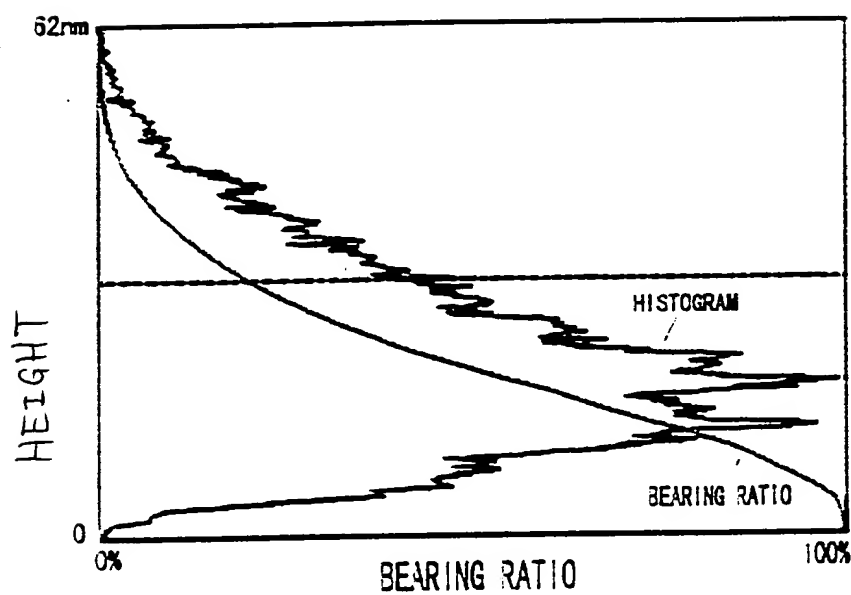


Fig. 3B

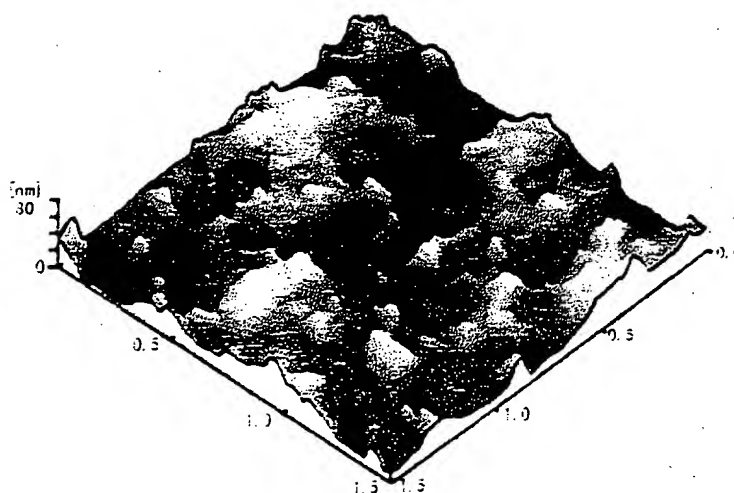
AFTER HIGH TEMPERATURE ANNEALING



BEFORE HIGH TEMPERATURE ANNEALING

20.0kV X50.0K 600um

AFTER HIGH TEMPERATURE ANNEALING



BEFORE HIGH TEMPERATURE ANNEALING

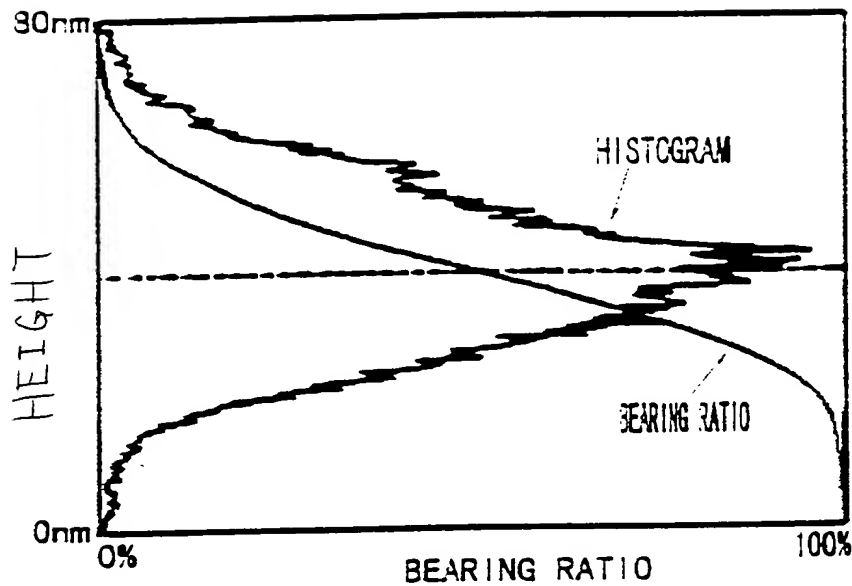


Fig. 15

AFTER HIGH TEMPERATURE ANNEALING

OBSERVATION REGION	BEFORE HIGH TEMPERATURE ANNEALING	AFTER HIGH TEMPERATURE ANNEALING
1	13.623	40.925
2	20.027	51.126
3	20.629	59.364
4	21.798	48.539
5	16.666	55.341
6	15.097	46.510
7	13.120	57.655
8	14.035	51.120
9	12.599	54.416
10	20.699	36.945
MINIMUM VALUE (%)	12.60	36.95
MAXIMUM VALUE (%)	21.80	59.36
AVERAGE VALUE (%)	16.83	50.19
STANDARD DEVIATION σ	3.61	7.18

Fig. 16

BEARING RATIO AT 2^{-1} (P-V VALUE) (%)